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What are Memelements: Memristor, Memcapacitor and Meminductor?

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ABSTRACT

Memory circuit elements with the moniker Memelements include memristor, memcapacitor and meminductor. These are newly proposed circuit elements whose electrical properties namely: memristance, memcapacitance and meminductance respectively, depend on their previous history of charge or flux associated to them. In other words, they are circuit elements with memory having huge potential to revolutionize electronic industries in various applications. These names are extension of the three existing fundamental circuit elements, namely resistor, capacitor and inductor respectively. This paper presents an insight into these memelements including their device technology, modelling and applications. To explore the signatures of these circuit elements, we derived their models and the corresponding responses are observed. The paper unravels the criticisms on the existence of memelements especially their classification as fundamental circuit elements. It is well established that memelements are not fundamental circuit elements but rather another set of elements potentially useful in bio-inspired networks, nonvolatile memory, chaotic systems, and many other applications.

Keywords: *Memelements · Memristor · Memcapacitor · Meminductor · Constitutive Relationship · Modelling · Criticisms · Applications*

1. Introduction

Electronic devices and systems are built using discrete components known as electronic components. Example of these components are resistors, capacitors, inductors, transistors, microchips, diodes, sources, etc. In terms of the causes and effects, electronic components are classified into active and passive circuit elements. Active circuit elements such as transistors, voltage and current sources, etc. are capable of generating an electric power (or power gain in the case of transistors) while passive circuit elements such as resistor, capacitor, inductor, etc. can only use, oppose or store the available power. In electrical and electronic engineering, resistor, capacitor and inductor are the three familiar fundamental passive circuit elements and they serve as the basic units in system design and implementation. The fundamental passive circuit elements do not give

out power, hence their associated power is always positive i.e. $P(t) \triangleq V(t)I(t) > 0$. However, in 1971, Leon Chua envisioned the existence of the missing fourth fundamental circuit element complementing resistor, capacitor and inductor [1]. The proclamation of memristor as the fourth missing circuit element can be observed from the tetrahedral symmetry in Figure 1a. Leon Chua argued that for the sake of completeness there must be a phenomenological constant defined by the missing relation between the magnetic flux linkage ϕ and the electric charge q, see Figure 1a. This phenomenological constant was named memristor (M), which basically means a memory resistor having electrical property as memory resistance (also knowns as memristance), measured in Ohms just like resistor.

Recall that the four familiar circuit variables in electrical and electronic engineering are the voltage (V), electric current (I), magnetic flux (ϕ) and electric charge (q). These circuit variables are related by the time derivatives $V(t) = \frac{d\phi(t)}{dt}$ and $I = \frac{dq(t)}{dt}$, or in the integral forms, respectively as:

$$\phi = \int_{-\infty}^{t} V(\tau)\, d\tau = \phi_0 + \int_{-0}^{t} V(\tau)\, d\tau, \tag{1}$$

and

$$q = \int_{-\infty}^{t} I(\tau)\, d\tau = q_0 + \int_{-0}^{t} I(\tau)\, d\tau, \tag{2}$$

where $\phi_0 = \int_{-\infty}^{0} V(\tau)\, d\tau$ and $q_0 = \int_{-\infty}^{0} I(\tau)\, d\tau$ are the initial flux and charge at time $t = t_0$. In fact, ϕ_0 and q_0 represent all the past history of $V(t)$ and $I(t)$ respectively, from time $t = -\infty$ to $t = t_0$. Moreover, t_0 refers to the initial time under consideration and it may be any intermediate time i.e. not necessarily be 0. For convenience, it is usually assumed that at infinite time (i.e. $-\infty < t \leq 0$): $V(t = -\infty) = 0V$ and $I(t = -\infty) = 0A$ such that $\phi_0 = 0Wb$ and $q_0 = 0C$. However, this is not always true especially in the case of memory circuit elements (to be defined shortly in the following) in which their electrical properties depend on the history of charge or flux associated with them. In fact, the initial values of charge and flux manifest significantly on the memory effect of the memory circuit elements. The initial charge q_0 was able to dramatically affect the circuit response of a memristor which in turn affect the dynamic and the steady state of a system [2]. Therefore, as shown in Figure 1a, there are altogether six possible relationships among the four circuit variables and the four circuit elements (including the memristor). These relationships are deeply explored by given their axiomatic definitions in section 3. Chua et al. have extended the concept of memristor to memristive systems with an effort to affirm the existence of memristor as the fourth passive circuit element and how memristive systems could be identified from other nonlinear dynamical systems [3]. This effort was to strengthen his argument amid growing criticisms.

The discovery of memristor (memory resistor) led to the generic concept of memory circuit elements (also known as Memelements) which includes other two newly proposed memory circuit elements, namely: memcapacitor and meminductor, a contractions of memory capacitor and memory inductor respectively [4, 5, 6, 7]. The definition of memelements include two more new variables, i.e. the time-integral of magnetic flux:

$$\rho = \int_{-\infty}^{t} \phi(\tau)\, d\tau,$$

and the time-integral of electric charge:

$$\sigma = \int_{-\infty}^{t} q(\tau)\, d\tau.$$

Figure 1b shows the relationships of the memelements with respect to their circuit variables. Initially, memelements were claimed to be fundamental circuit elements just like resistor, capacitor and inductor, however this assertion has faced strong oppositions which would be mentioned in this paper. As already explained, resistor, capacitor and inductor are the three familiar basic or fundamental passive circuit elements, and it happens that memelements reflect the memory effects of the three existing fundamental circuit

elements, hence the name memory circuit elements. This can be confirmed by the disappearance of their pinched hysteresis loop as the applied input frequency tends to infinity, which results in their response to resemble that of the three fundamental circuit elements, accordingly. To prove this explanation, we show the effect of varying the input frequency for each of the memelements.

There are similarities between the fundamental circuit elements and the memelements, for example, the deductive-like expressions and same units of measurements which questioned their fundamental claims. Here, the term fundamental refers to exist independently which cannot be realized by a simple combination of other basic circuit elements. However, the port variables of each memelement are also the port variables of its parent element, that is, (resistor and memristor), (capacitor and memcapacitor) and (inductor and meminductor). This relational-dependency questioned the existence of memelements as separate and independent fundamental circuit elements. Therefore, to explore these similarities in terms of relational-dependency, we present the periodic table of circuit elements which clearly shows the evolution of the circuit elements with respect to the given circuit variables.

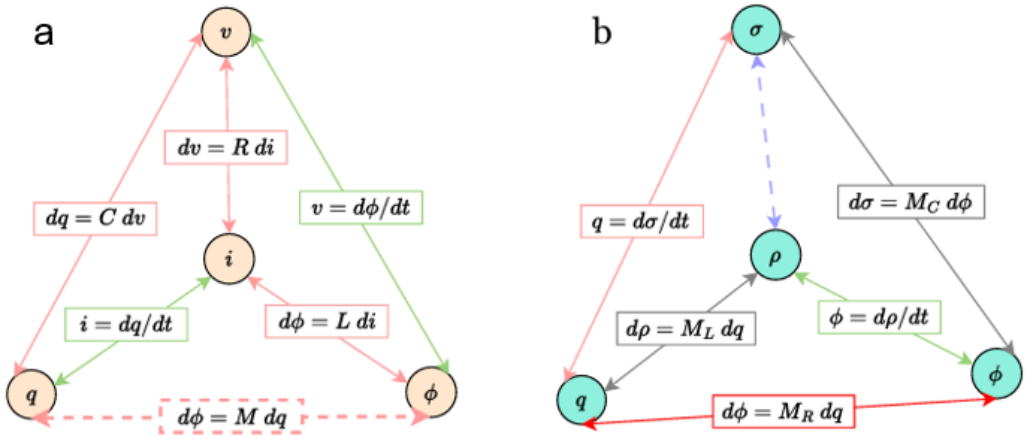

Figure 1: Circuit variables and their relationships with fundamental circuit elements. (a) Tetrahedral symmetry of the fundamental circuit elements and the claim of the missing memristor M. (b) Relationships of memelements with respect to their circuit variables.

From Figure 1b, the constitutive relationships between the pair of the variables q, ϕ, σ and ρ give the definitions of the memelements illustrated as follows:

- $d\phi = M_R \cdot dq$: Memristor.
- $d\sigma = M_C \cdot d\phi$: Memcapacitor.
- $d\rho = M_L \cdot dq$: Meminductor.

Where M_R, M_C and M_L are the memristance, memcapacitance and meminductance, and these are the electrical properties of memristor, memcapacitor and meminductor respectively.

This paper helps to better understanding of these circuit elements by describing details of their modelling techniques, the efforts toward their physical device realization and further unravels the criticisms of memelements regarding their claims as fundamental circuit elements. It also further demonstrates why there is huge interest in the scientific discovery of memory circuit elements owing to their potential relevance in response to the contemporary technological challenges in areas such as nano-technology, neuromorphic systems, high density memory applications, etc. We strongly believed that the contents of this paper will be of great interest to engineers and researchers working in the field of memristive, memcapacitive and meminductive systems, and to those who are interested to start working in this field.

2. Memristor proclamation and its discovery

Memristor can be identified from other nonlinear systems by observing its typical circuit response, also known as its fingerprints [8, 9]. The prominent fingerprint of a memristor is the pinched hysteresis loop in its current-voltage (I-V) plane which shrinks to a linear graph as the frequency of the applied input signal tends to infinity. There are many natural phenomenon (such as in biology, mercury lamp, solid state devices, etc...) with occurrences of pinched hysteresis loop in their I-V graphs, however no efforts to classify such phenomenon as memristors because there were not many thoughts on the conception of the fourth basic passive circuit element [10]. Another possible reason for the absentee of memristor is that it is a nano device and can only be realized by matured nano technology and this technology is not available some decades ago [11]. Although the existence of memristor was proclaimed in 1971 [1], however, it was only realized in 2008 by researchers of HP laboratory, in which each junction of their nanoscale crossbar array experiment showed the typical outlined characteristics of a memristor [12, 13], see Figure 2. However, this is not the first time such behaviour was observed, thus causes doubtful and oppositions in the HP's claimed discovery of memristor. Memelements are intrinsically asymmetric, hence their response is affected by the polarity of the applied input source [14, 15]. As shown in the memristor symbol of Figure 2, the darker edge corresponds to the lower potential terminal, meanwhile the unmarked edge is the higher potential terminal. This notation is also applicable to both memcapacitor and meminductor. Extensive study of the polarity reversal effects of a memristor is presented in [14].

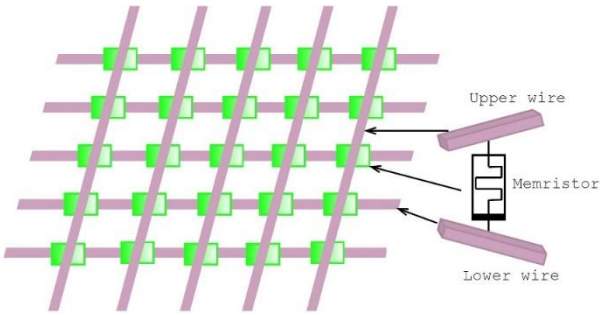

Figure 2: Crossbar arrays in which each junction forms a memristor.

Let start by briefly giving the mathematical concept of memristor before addressing the claimed memristor discovery in Figure 2. A voltage V applied to a device will establish the flow of current I through it, likewise, an applied current will establish voltage across such device. Hence, V and I are complementary pair, as will be detailly explained in sections 3 and 4. Depending on the type of the applied input signal to a memristor, it can be a charge-controlled memristor if the input to the memristor is a current source and a flux-controlled memristor when the input is a voltage source. The constitutive relation of a charge-controlled memristor is expressed as $\phi = \hat{h}(q)$ and it is a differentiable function of q. The constitutive relationship of a circuit element can be transformed to give its corresponding port relationship. Therefore, differentiating both sides with respect to time, it becomes:

$$\frac{d\phi}{dt} = \frac{d}{dt}\left(\hat{h}(q)\right) \Rightarrow \frac{d\phi}{dt} = \frac{d\hat{h}(q)}{dq}\frac{dq}{dt}, \tag{3}$$

where $M(q) = \frac{d\hat{h}(q)}{dq}$ is the charge-controlled memristance. Equation (3) shows the port relation of an ideal charge controlled memristor i.e. $V(t) = M(q)\, I(t)$, in which the state variable of the system is only the function of the flowing charge through it. However, the general expression of a memristor is a state-dependent Ohm's law relationship. Hence the generalized expressions of a charge-controlled memristive systems are expressed by the following set of equations [16]:

$$\begin{cases} V(t) = M(x, I, t)\, I(t) \\ \dfrac{dx}{dt} = f(x, I, t), \end{cases} \tag{4}$$

where x is the vector representing the internal state variable of the system and $f(x, I, t)$ is function describing the evolution of x. Notice that M is a response function and it depends on both the internal state x and the flowing current $I(t)$. Here, $I(t)$ is the independent variable which causes a voltage $V(t)$ to be dropped across the memristor. An ideal charge-controlled memristor is a subset of equation (4) in which the function in the state equation reduces to $f(I, t)$ such that $x = \hat{f}(q)$, and it can be expressed as:

$$\begin{cases} V(t) = M(q)\, I(t), \\ \dfrac{dq}{dt} = I(t). \end{cases} \tag{5}$$

Moreover, the constitutive relation of a flux-controlled memristor can be expressed in the form $q = \hat{g}(\phi)$, and it is a differentiable function of ϕ. Thus, differentiating this expression with respect to time, it becomes:

$$\frac{dq}{dt} = \frac{d}{dt}\big(\hat{g}(\phi)\big) \Rightarrow \frac{dq}{dt} = \frac{d\hat{g}(\phi)}{d\phi}\frac{d\phi}{dt}, \tag{6}$$

where $\mathcal{M}(\phi) = \frac{d\hat{g}(\phi)}{d\phi}$ is the flux-controlled memductance in Siemens and it is also known as the inverse-memristance M^{-1}. Likewise, the generalized expression of a flux-controlled memristor becomes:

$$\begin{cases} I(t) = \mathcal{M}(x, V, t)\, V(t), \\ \dfrac{dx}{dt} = g(x, V, t). \end{cases} \tag{7}$$

Here, x is also the internal state variable of the system and $g(x, V, t)$ is function describing its dynamic. The independent source is a voltage $V(t)$ and the memductance $\mathcal{M}$ depends on the internal state variable x and the voltage $V(t)$. Notice here that the state variable x is a function of the flux ϕ, hence equation (7) characterizes a flux-controlled memristor. However, if the state variable x depends only on the flux as the case of a flux-controlled memristor, the function in the state equation (7) reduces to $g(V, t)$ such that $x = \hat{g}(\phi)$. Therefore, an ideal flux-controlled memristor is a subset of equation (7) and it can be expressed by the following set of equations:

$$\begin{cases} I(t) = \mathcal{M}(\phi)\, V(t), \\ \dfrac{d\phi}{dt} = V(t). \end{cases} \tag{8}$$

Memristor modelling is one of the many interesting research areas about memristor, and it helps to emulate the behavioural characteristics of a memristor through simulation. Recall that memristor is a new circuit element, hence it is important to understand how it will respond in a circuit prior to implementation. The models of memristor allow to simulate memristor-based circuits and carry out all the necessary analysis and observations, which helps to gain an insight knowledge of a targeted design. Moreover, memristor chips are expensive and are not readily available, hence it is more flexible to get started with a memristor model. Self-Directed Channel (SDC) memristor chips are commercially available online by KNOWM Inc. [17]. Unlike the TiO_2 memristor, SDC memristors achieve their resistive switching by the formation and dissolution of a conducting channel filament. One of the widely used memristor models is the TiO_2 model whose mathematical description was deduced from the schematic illustration in Figure 3 [12].

Figure 3a shows the fabrication of TiO_2 memristor, and it consists of a thin film of TiO_2 sandwiched between two platinum electrodes. One edge of the thin film layer of TiO_2 is slightly doped with oxygen vacancies allowing the doped region to have lower resistance, in other words to be more conductive, meanwhile the undoped region remain less conductive due to its higher resistance. After electroforming process, the oxygen vacancies are localized, thus creating an imaginary boundary between the doped and the undoped regions, see figure 3a. This imaginary boundary moves back and forth depending on the magnitude and direction of the flowing charge through the device, thus allowing the device to have variable resistance. The arrangement resembles a potentiometer whose setting is determined by the instantaneous charge $q(t)$ flowing through the device. Hence the arrangement can be modelled to have two resistances, namely: R_{on} the

least value of resistance when the device is fully conducting (ON state) and it corresponds to the resistance of the doped region, and R_{off} is the highest value of the resistance when the device is less conducting (OFF state) and it corresponds to the resistance of the undoped region. Recall that the resistance of the device is not fixed and it always transits between the two limiting resistance state (R_{on} and R_{off}). Hence, the instantaneous resistance (also known as memristance in this case) is determined by the state variable of the system. Therefore, the notation in Figure 3b shown that $R_{on}^{*} = \frac{w}{D} R_{on}$ is the instantaneous resistances at the doped region, meanwhile $R_{off}^{*} = \left(1 - \frac{w}{D}\right) R_{off}$ is the instantaneous resistance at the undoped region. The cumulative effect gives the instantaneous memristance: $M(w) = \frac{w}{D} R_{on} + \left(1 - \frac{w}{D}\right) R_{off}$ and the state equation characterizing the dynamic of the memristance was obtained to be $\frac{dw}{dt} = \frac{\mu_v R_{on}}{D} I(t)$. Here, w is the state variable of the system, μ_v is the mobility of charge carriers and D is the width of the sandwiched layer of TiO_2 film. However, considering a normalized state variable $x = \frac{w}{D}$, the set of equations modelling the characteristic of Figure 3 become:

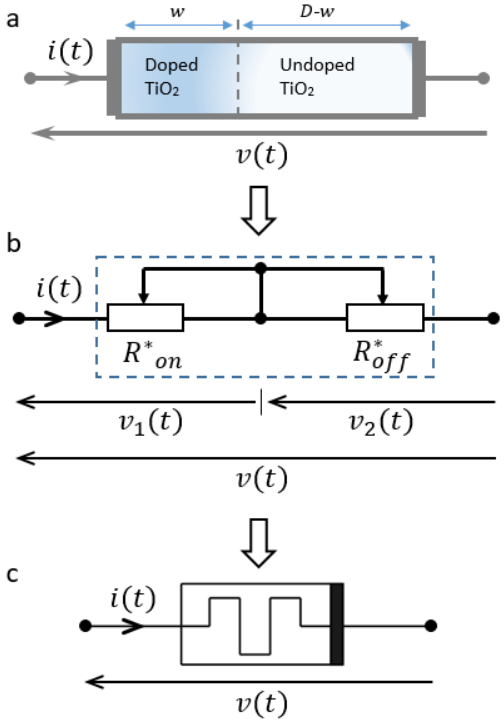

Figure 3: Schematic of TiO_2 memristor. (a) Fabrication, (b) Modeling and (c) Symbol.

$$\begin{cases} V(t) = M(x)\, I(t), \\ \dfrac{dx}{dt} = \dfrac{\mu_v\, R_{on}}{D^2} I(t), \\ M(x) = (1 - x)\, R_{off} + R_{on}\, x. \end{cases} \tag{9}$$

Since D is the entire width of TiO_2, then $w \in [0, D]$. It implies that $x \in [0,1]$ and $M \in [R_{off}, R_{on}]$. Therefore, integrating the state equation in (9) for x from 0 to 1, it becomes:

$$\int_0^1 dx = \frac{\mu_v\, R_{on}}{D^2} \int_0^t I(t)\, dt \Rightarrow\ q = \frac{D^2}{\mu_v\, R_{on}} = Q_D,$$

where Q_D is the charge scaling factor necessary for switching between R_{on} (ON state) and R_{off} (OFF state). Hence, the equation set (9) becomes:

$$\begin{cases} V(t) = M(x)\, I(t), \\ \dfrac{dx}{dt} = \dfrac{1}{Q_D} I(t), \\ M(x) = R_{off} - \delta R\, x, \end{cases} \tag{10}$$

where $\delta R = R_{off} - R_{on}$. Equation (10) is a bipolar model of charge-controlled memristor because it requires both positive and negative polarity of the applied signal to switch its resistance from R_{on} to R_{off} and vice versa. Other memristors can be unipolar or nonpolar because their memristance transition from R_{on} to R_{off} and vice versa occurs at the same voltage polarity [18, 19, 20, 21, 22, 23]. The state equation in (10) is solved to give the explicit expression of the state variable as follows:

$$x = x_0 - \frac{q_0}{Q_D} + \frac{1}{Q_D} q(t), \tag{11}$$

where x_0 is the initial coordinate of the state variable when the last amount of charge flowed through the device at time $t = t_0$ is q_0. The memristance expression becomes:

$$M(q) = M_0 - \frac{\delta R}{Q_D} q(t), \tag{12}$$

Where $M_0 = R_{off} - \delta R \left(x_0 - \frac{q_0}{Q_D}\right)$ is the initial memristance at time $t = t_0$ and the port equation is as expressed in equation (10). Normally, $R_{off} \gg R_{on}$, hence $\delta R \approx R_{off}$. Therefore, if $q_0 \ll Q_D$, then $M_0 \approx R_{off}$. For example, consider a sinusoidal applied current source as $I(t) = I_0\, sin\, (\omega t)$, then the corresponding expression for the variable $q(t)$ becomes $q\,(t) = \frac{I_0}{\omega}\left(1 - cos\,(\omega t)\right)$. Notice here that for the time window $[-\infty, 0]$, it is assumed that $q(0) = \int_{-\infty}^{0} i(\tau)\; d\tau = 0$. Figure 4 shows the corresponding results for $R_{off} = 16K\Omega$, $R_{on} = 100\Omega$, $D = 10nm$ and $\mu_v = 10^{-14} V.s/m^2$, which gives $Q_D = 100\mu C$. The state equation in (10) shows a linear relation between the coordinate of the state variable x and the time integral of $I(t)$ (or the charge) as shown in equation (11). Hence, memristor remembers the history of charges flowed through it. If the device is partially doped, then $x \approx 0$. However, if the device is wholly doped, $x \approx 1$. Figure 4a shows the typical current-voltage waveform of a memristor. The waveforms are in phase but one of them is always skewed and the traces manifest the nonlinear nature of a memristor. Figure 4b shows the corresponding pinched hysteresis loop. Meanwhile, Figures 4c and 4d show the flowing charge and the corresponding memristance transition, respectively.

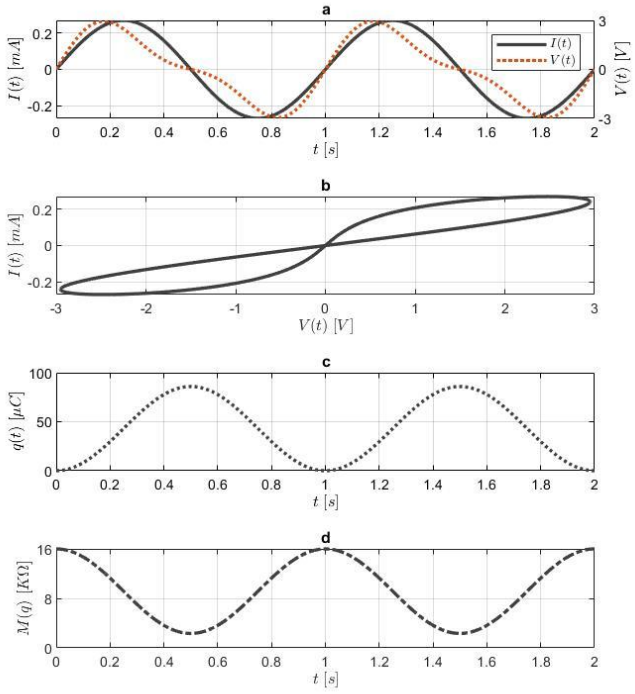

Figure 4: The typical response of a memristor. (a) current-voltage waveform, (b) current-voltage characteristic i.e. pinched hysteresis loop, (c) the flowing charge $q(t)$ through the memristor and (d) the corresponding time-evolution of the memristance $M(q)$.

As demonstrated in Figure 4, the charge flowing through the memristor is $q\,(t) = \frac{I_0}{\omega}\,\big(1 - cos\,(\omega t)\big)$. For a fix value of the current amplitude I_0, the flowing charge $q(t)$ is affected by the applied input frequency ω and the inversely proportional. Hence, as the input frequency increases, the flowing through the memristor decreases, and vice versa. From equation (12), it can be clearly seen that the memristance $M(q)$ is directly proportional to $q(t)$ but not in the sense that $M(q)$ increases as $q(t)$ increases, and vice versa. Recall that the model has two limiting resistance values R_{off} and R_{on} and the memristance $M(q)$ always transits within these values. Obviously, high resistance implies low flowing charge and low resistance accounts to high flowing charges, as explained in the formed imaginary boundary illustrated in Figure 3a. Hence, it follows that as the flowing charge $q(t)$ increases, then $M(q)$ decreases and transits toward R_{on}. Conversely, as $q(t)$ decreases, then $M(q)$ increases and transits toward R_{off}. This is confirmed by the evolution of $q(t)$ and $M(q)$ in Figures 4c and 4d respectively. Therefore, it should be clearly understood that according to equation (12) $M(q)$ is directly proportional to $q(t)$ but the transitioning of $M(q)$ between R_{off} and R_{on} depends on the quantity and direction of the flowing charge through the memristor.

Furthermore, since $q(t)$ is affected by the variation of the applied input frequency, then it also affected $M(q)$. Therefore, as w ↑, then $q(t)$ ↓ and $M(q)$ ↑, and when w ↓, then $q(t)$ ↑ and $M(q)$ ↓. The up (↑) and down (↓) arrows represent increase and decrease respectively. Therefore, it is because of this reason that the lobe area in the pinched hysteresis loop of memelements is significantly affected by the variation of the input frequency. It causes the shrinkage of the lobe area as the input frequency increases. Figure 5 shows the effect of varying the input frequency on the I-V characteristic of a memristor. It shows that as the input frequency increases, the pinched hysteresis loops shrink to a linear graph resembling a linear resistor. If the initial charge q_0 is very small, then the initial memristance M_0 becomes approximately R_{off}. Thus, the R_{off} slope remain barely fixed and the R_{on} slope varied, as can be confirmed from the variable term $\frac{\delta R}{Q_D} q(t)$ in equation (12). Figure 5 illustrates the three prominent signatures of a memristor. At infinite input frequency, the lobe area disappears and I-V characteristic of memristor resembles ordinary linear resistor. It is worth to note that the lobe area is the manifestation of the hysteretic effect, hence the memory effect. The disappearance of the lobe area means the absent of the memory which differentiate a memristor from ordinary linear resistor. Therefore, one will ponder whether memristor at infinite input frequency is something different from ordinary linear resistor.

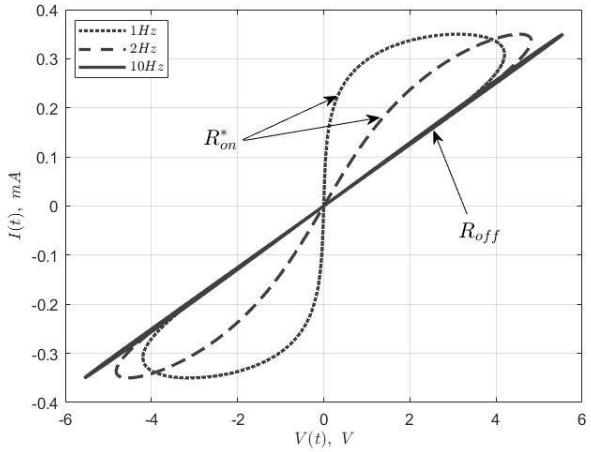

Figure 5: Effect of change in the input frequency on the I-V characteristic of a memristor.

The state equation modelled the charge carriers drifting between the coordinates 0 and 1 and it does not take into account the case $x = 0$ or $x = 1$. Hence, equation (10) is called a linear dopant drift model. The coordinate switching transition from $x = 0$ to $x = 1$ and vice versa, corresponds respectively, to the memristance transition from R_{off} to R_{on} and vice versa. To facilitate the memristance transition at the

boundaries and maintaining the state variable within the interval [0,1], a window function $f(x)$ is added to the right-hand side of the state equation in (10), thus imposing a nonlinear dopant drift at the boundaries [24]. The set of equations become:

$$\begin{cases} V(t) = M(x_R)\, I(t), \\ \dfrac{dx_R}{dt} = \dfrac{1}{Q_D} f(x)\, I(t), \\ M(x) = R_{off} - \delta R\, x, \end{cases} \tag{13}$$

The state equation in (13) characterizes a nonlinear dopant drift model. There are many proposed window functions $f(x)$ for nonlinear dopant drift modeling [25]. The window function lacks physical meaning because it is simply added to avoid the model computational issues at the boundaries experience in the linear model when the applied input signal is substantially enough to force the state variable to approach 0 or 1. These particular issues are extensively discussed, including the proposed new model with no boundary issues and it does not require a window function [24].

William et al. have claimed to have found the missing memristor based on the information in Figure 2 and the modelling equations (10) and (13). Although their findings displayed the typical characteristics of memristor but there is outcry on the scientific merit of their claimed discovery [26]. The TiO_2 memristor can be categorised as a resistive switching device and there are many such devices in the literature even showing similar characteristics and they were never claimed to be memristor. In fact, Suresh et al. have argued that their findings were similar with the ones by William et al., inciting that their finding must be memristor too [27]. Hence, many other criticisms on memristor as basic circuit elements are addressed in section 8. The claimed discovery of HP TiO_2 memristor sparked interest on memristor and many other possible fabrication technologies. The fabrication technologies of memristor are based on magnetic and ionic effects [25]. In the following section 3, we further present the axiomatic definitions of the three known fundamental circuit elements which allows to weigh the claim of memristor as the fourth fundamental circuit element.

3. The axioms of the fundamental circuit elements

Electrically, resistance (R) refers to the inherent property of a material to resist the flow of electric charges through it and this is due to the collisions of charge carriers as the they drift from one point to another by the application of potential difference. Thus, it causes some of the power to be dissipated as heat. By virtue of this, resistor is considered as the fundamental passive circuit element. The resistance R of a material depends on its resistivity ($\mathcal{R}$) which also depends on many other factors, such as temperature. The classical Ohm's law proves the constitutive relation of a resistor between the applied potential difference (V) and the established flowing current (I) as $V = R \cdot I$, where the dot $\cdot$ represents a multiplication symbol. Furthermore, an electric field is created between two conducting wires or plates separated by a medium (such as dielectric) due to the accumulated surface charges. Capacitance C refers to the electrical characteristics that signify the amount of charge q stored between two conducting materials due to the application of potential difference V. The stored charges is proportional to the applied potential difference, hence it is characterized by the relation $q = C \cdot V$. This electrical property suggests that capacitor is a fundamental passive circuit element and it stores energy in the form of electric field. Lastly, a current-carrying conductor or wire is always associated with a magnetic field whom strength depends on the magnitude of the flowing current and the nature of the conductor i.e. loop or coil (air or solid core). Application of Faraday's and Lenz's laws showed that as the flowing current varies, the associated magnetic flux also varies, thus induces a voltage which acts to oppose itself to any change in the current that produces it i.e. $V(t) = -L\frac{dI(t)}{dt}$ or $\phi = L \cdot I$. Therefore, inductance refers to the electrical property of an inductor to oppose to a change in electric current flowing through it and it stores energy in the form of magnetic field. This peculiar behaviour suggests that inductor is a fundamental circuit element. Therefore, these three circuit elements happened to be fundamental by their nature.

For over a century, resistor, capacitor and inductor are considered the three basic passive circuit elements owing to their fundamental existence. However, using the tetrahedral symmetry argument illustrated in Figure~1a for the missing relation between ϕ and q, Leon Chua proclaimed the existence of memristor and he categorized it as the fourth basic passive circuit element [1]. The constitutive relation of the memristor relates the magnetic flux and electric charge. The electric charge and the magnetic flux are not variables that can be measured externally, but rather an integral variable of current and voltage respectively, perhaps this causes memristor to remain unexplored. Let observe the current-voltage responses of these circuit elements. Consider a black box (which is a Device Under Test - DUT) constituting a one port network as shown in Figure 6. The applied voltage across the DUT is $V(t)$ which also establishes a current $I(t)$ flowing through it. The DUT can be any bilateral or non-bilateral two terminal circuit elements, for example: resistor, diode, capacitor, etc. The current-voltage response also known as the I-V characteristic characterizes the DUT as a specific type of circuit element. For decades, the I-V characteristic is one of the leading methods used for components characterization and identification, including circuit components having more than two terminals such as transistor. Furthermore, the I-V characteristic can be used to classify circuit elements as linear or nonlinear. The DUT can be a resistor, a capacitor or an inductor, each having electrical property as resistance R, capacitance C and inductance L respectively, connected across a sine input voltage source $V(t) = V_0\ sin\ (\omega t)$, where V_0 and $\omega = 2\pi f$ are voltage amplitude and input frequency respectively.

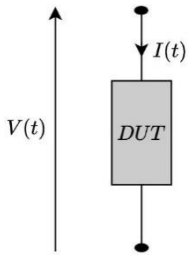

Figure 6: One port network as a device under test (DUT).

If the DUT is a resistor, the port equation is expressed as $V(t) = R \cdot I(t)$ and the I-V characteristic is a linear graph as shown in Figure 7a. The value of the resistance is determined by the slope of the graph. Note that the resistor can be nonlinear as well, such as the cubic resistance in Fitzhugh Nagumo model. However, nonlinear resistors are not fundamental because linearity is essential in assessing the fundamental nature of a resistor. This is also true in the case of capacitor and inductor. The electrical property of resistor, capacitor and inductor is affected by many factors, such as temperature, frequency, etc. Under normal conditions of operation, these circuit elements are classified as linear element, hence their port relations indicate linear relationships. If the DUT is a capacitor, the port equation becomes $I = C\frac{dV(t)}{dt}$ and the I-V characteristic is a circle as shown in Figure 7b. Note the trajectory direction (indicated by an arrow) of the locus due to the fact that $X_C = \frac{1}{j\omega C}$, where X_C is capacitive reactance in Ohms. Meanwhile, if the DUT is an inductor, the port equation is expressed as $V(t) = L\frac{dI(t)}{dt}$ and the I-V characteristic is shown in Figure 7c and it is also a circle, however the trajectory direction of the locus is opposite to that of the one in capacitor because $X_L = j\omega L$, where X_L is the inductive reactance in Ohms. Moreover, if the DUT is a memristor, the I-V response is a pinched hysteresis loop as shown in Figure 7d. The model used for the production of Figure 7d is given by equation (10).

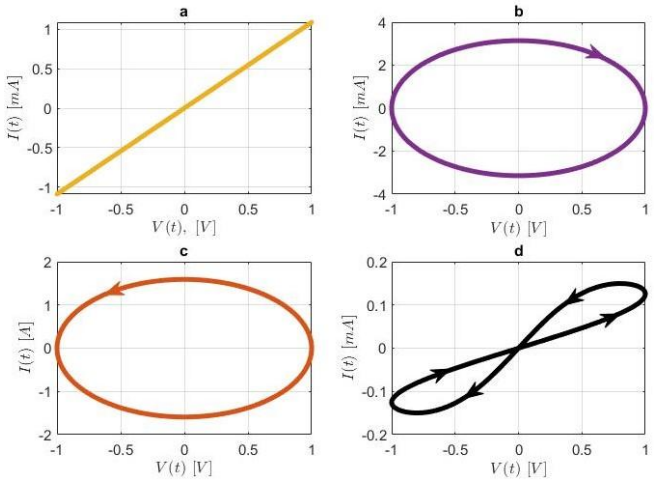

Figure 7: The typical I-V characteristics of the three fundamental passive circuit elements and the memristor. (a) Resistor, (b) Capacitor, (c) Inductor and (d) Memristor.

Although resistor, capacitor and inductor, to some extent could be simplified as linear circuit elements, memristor is characterized as nonlinear circuit element [1]. Simplistically, the nonlinearity of a memristor can be observed from its typical current-voltage waveforms as illustrated in Figure 8. The upper and lower panes of Figure 8 are the current-voltage waveform and the I-V response respectively. In memristor, $V(t)$ and $I(t)$ are always in phase, hence the labels 1, 3 and 5 are the points where $V(t) = 0V$ and $I(t) = 0A$, meanwhile the labels 2 (for $V(t)$) and 2* (for $I(t)$), and 4 (for $V(t)$) and 4* (for $I(t)$) correspond to their positive and the negative peak values respectively. While the voltage increases up to the maximum (Point 2 of the upper pane i.e. Figure 8a) at $0.25s$, the current also increases upto the maximum (point 2*) at $0.37s$. Hence, observing the time window $[0.25s, 0.37s]$, it can be seen that while the voltage is decreasing, the current is still increasing and this is a sign of nonlinearity. Similar behavior is observed during the negative half cycle. This behavior also manifested in the corresponding I-V response shown in the lower pane i.e. Figure 8b. Hence, Figure 8b shows that for every value of $V(t)$ there is corresponding two values of $I(t)$ except at the origin where both $V(t)$ and $I(t)$ are pinched i.e. $V(t) = 0V$ and $I(t) = 0A$.

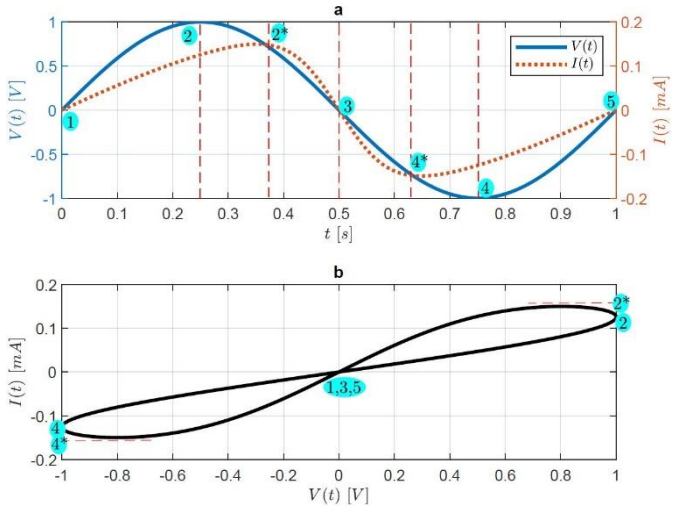

Figure 8: The response of memristor depicts a nonlinear circuit element.

Memelements are nanoscale devices whose electrical properties depend on the history of the system. At nanoscale, small voltage generates large electric field, hence memelements tend to have common dynamical

properties of charge carriers (electrons or ions). Hence, they have pinched hysteresis loop in the first and third quadrants of the Cartesian plane of their constitutive relationships, that is:

- $V = M_R(x) \cdot I \Rightarrow I$ versus V for the memristor, with $x = \hat{f}(q)$.
- $q = M_C(x) \cdot V \Rightarrow q$ versus V for the memcapacitor, with $x = \hat{f}(\sigma)$.
- $\phi = M_L(x) \cdot I \Rightarrow I$ versus ϕ for the meminductor, with $x = \hat{f}(\rho)$.

The state variable x differs for each model and it depends on the constitutive variables for each model under consideration. Given the voltage and current responses, it may be enough to identify a particular device or component. Similar approach is followed by Chua et al. to identify memelements from their current-voltage responses and constitutive relationships [5]. Secondly, given the model of a particular device, it can be identified or validated by observing its typical response.

4. Periodic table of circuit elements and the Memelements

Each pair of the four circuit variables constitutes what is known as the *constitutive relationship (CR)* and it characterizes the attributes of the circuit element in which they are applied. Here, the attribute refers to a phenomenological constant which characterizes the electrical property of the circuit element under consideration. The generalized expressions for the voltage and current signals applicable to a one port device can be expressed as [28]:

$$V^{(\alpha)} \triangleq \begin{cases} \dfrac{d^{\alpha}V(t)}{dt^{\alpha}}, & if\ \alpha > 0 \\ V(t), & if\ \alpha = 0 \\ \displaystyle\int_{-\infty}^{t}\int_{-\infty}^{\tau_2}\cdots\int_{-\infty}^{t-\alpha} V(\tau_{-\alpha})d\tau_{-\alpha}d\tau_{-\alpha-1}\cdots d\tau_1, & if\ \alpha < 0 \end{cases} \tag{14}$$

and

$$I^{(\beta)} \triangleq \begin{cases} \dfrac{d^{\beta}I(t)}{dt^{\beta}}, & if\ \beta > 0 \\ I(t), & if\ \beta = 0 \\ \displaystyle\int_{-\infty}^{t}\int_{-\infty}^{\tau_2}\cdots\int_{-\infty}^{t-\beta} V(\tau_{-\beta})d\tau_{-\beta}d\tau_{-\beta-1}\cdots d\tau_1, & if\ \beta < 0 \end{cases} \tag{15}$$

where $V^{(\alpha)}$ and $I^{(\beta)}$ are the constitutive variables denoting terminal voltages and currents respectively, meanwhile α and β are any integers (i.e. positive, zero or negative) denoting the orders of the derivatives or integrals with respect to time of the terminal voltages and currents for the element under consideration. If the voltage $V(t)$ is applied to a one port device, the current $I(t)$ flowing through it can be measured. Similarly, if a current $I(t)$ is applied to a one port device, the voltage $V(t)$ across it can be measured. Hence, $V^{\alpha}(t)$ and $I^{\beta}(t)$ are complementary signal pair and the *CR* can be expressed as $f(V^{\alpha}, I^{\beta}) = 0$ or in other words:

$$V^{\alpha}(t) = \hat{f}\left(I^{\beta}(t)\right)\ or\ I^{\beta}(t) = \hat{g}\left(V^{\alpha}(t)\right). \tag{16}$$

The functions $f()$, $\hat{f}()$ and $\hat{g}()$ model the current or voltage associated to any circuit element. Given all the possible values of α and β as illustrated in the α-β plane shown in Figure 9, then each coordinate corresponds to a particular one port circuit element. Hence, all the elements determine from the α-β plane are called (α,β) elements and the α-β plane is also known as the *periodic table of circuit elements* [28]. The (α,β) elements are also called higher order elements (HOEs) as they are very useful in modeling processes and very complex nonlinear dynamical systems [29, 30].

The periodic table of circuit elements (Figure 9) shows all the possible species of two-terminal (α,β) elements. The elements belonging to the same family appeared diagonally. Hence, elements with resistance property are in the R diagonal and they include resistor (R) and memristor (M_R) with (α,β) coordinates as (0,0)

and $(-1,-1)$ respectively. Here, the constitutive variables of resistor are (V^0, I^0) i.e. voltage and current. The (α,β) coordinate for the memristor $(-1,-1)$ signifies (V^{-1}, I^{-1}) which are the time-integrals quantities of its terminal voltage and current, which corresponds to flux and charge respectively, as its constitutive variables.

The (α,β) elements with inductance property are in L diagonal, thus including inductor (L) and memory inductor (meminductor, M_L) having coordinates $(-1,0)$ and $(-2,-1)$ respectively. The (α,β) coordinate of inductor $(-1,0)$ signifies (V^{-1}, I^0), hence its constitutive variables include its terminal current and the time-integral of its terminal voltage. However, the (α,β) coordinate of the meminductor $(-2,-1)$ signifies (V^{-2}, I^{-1}), hence its constitutive variables are the double integral of its terminal voltage and integral of its terminal current. Note that the double integral of voltage is simply the integral of magnetic flux. In other words, the constitutive variables of meminductor are the charge and the time-integral of flux.

Furthermore, the (α,β) elements with capacitance property are in C diagonal which includes capacitor (C) and memory capacitor (memcapacitor, M_C) having coordinates $(0,-1)$ and $(-1,-2)$ respectively. The (α,β) coordinate of capacitor $(0,-1)$ signifies (V^0, I^{-1}) which means that the constitutive variables include its terminal voltage and the time integral of its terminal current. Meanwhile, the (α,β) coordinate of memcapacitor $(-1,-2)$ signifies (V^{-1}, I^{-2}), therefore, the constitutive variables of memcapacitor include the time integral of its terminal voltage and the double integral of its terminal current. The double integral of current is simply the integral of charge. Hence, the constitutive variables of memcapacitor are the flux and the time integral of electric charge. The periodic table of circuit element also shows the possible existence of other two-terminal (α,β) elements including negative resistance. However, this paper focuses only on memelements. Exploring the potential of (α,β) elements is important owing to the growing interest in electronic systems modeling. Recently, an effort is made to reformulate theorems for demonstrating and observing all the possible pinched hysteresis loop that can be generated by an arbitrary (α,β) elements [30].

It follows from Figure 9 that the port variables of memelements are the corresponding time integrals of the port variables of their parent elements. These integrals take into account their previous and current states, perhaps it explains why memelements element reflects the memory of their parent element. The memory effect is manifested by the lobe area of the pinched hysteresis loop in the governing plane of the constitutive variables of their parent elements.

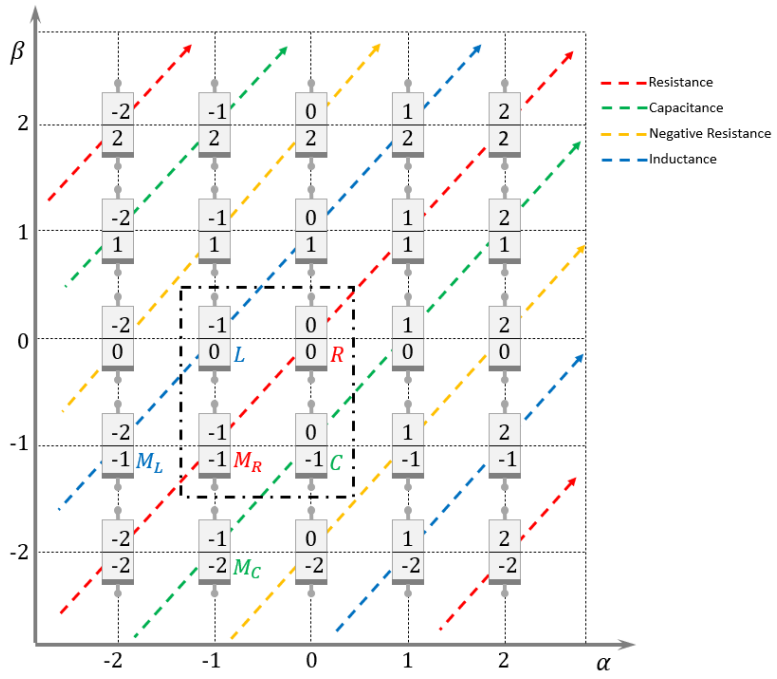

Figure 9: Periodic Table of circuit elements (also known as the (α,β) elements).

5. Memcapacitor

Recall that the constitutive relation of a capacitor C is given by $q = C\,V$ (or $dq = C\,dV$). Therefore, differentiating both sides with respect to time gives:

$$I(t) = \frac{dq}{dt} = \frac{d}{dt}\{CV\}. \tag{17}$$

The current-voltage relationship of a capacitor depends on the state of the capacitance, that is, whether the capacitance is fixed or time-varying. For a fixed capacitance, the current voltage relationship is expressed from equation (17) as:

$$I(t) = C\frac{dV(t)}{dt},$$

and for time-varying capacitance, equation (16) becomes:

$$I(t) = C\frac{dV(t)}{dt} + V(t)\frac{dC}{dt}.$$

An example of the time-varying capacitance is the membrane capacitance in biomimetic systems [31, 32, 33].

Memcapacitor is the contraction of memory capacitor, which simply means, a capacitor with memory whom capacitance (or elastance) depends on the history of the voltage across its two terminals (or charge flowing through it). As shown in figure 1b, memcapacitor is defined by the constitutive relationship between the variables σ and ϕ. Therefore, depending on the type of excitation, there are voltage-controlled and charge-controlled memcapacitors. A voltage-controlled memcapacitor can be expressed by the differential function: $\sigma = \hat{\sigma}(\phi)$. Differentiating both sides of this equation, it becomes:

$$\frac{d\sigma}{dt} = \frac{d}{dt}\big(\hat{\sigma}(\phi)\big) = \frac{d\hat{\sigma}(\phi)}{d\phi}\frac{d\phi}{dt}, \tag{18}$$

where $M_C(\phi) = \frac{d\hat{\sigma}(\phi)}{d\phi}$ is the memcapacitance. Notice that equation (18) corresponds to the port relation of a voltage-controlled memcapacitor: $q = M_C(\phi)\,V$. Likewise, a charge-controlled memcapacitor can be expressed by the differential function: $\phi = \hat{\phi}(\sigma)$. Differentiating this equation with respect to time, it becomes:

$$\frac{d\phi}{dt} = \frac{d}{dt}\Big(\hat{\phi}(\sigma)\Big) = \frac{d\hat{\phi}(\sigma)}{d\sigma}\frac{d\sigma}{dt}, \tag{19}$$

where $\mathcal{M}_C(\sigma) = \frac{d\hat{\phi}(\sigma)}{d\sigma} = M_C^{-1}$ is the inverse-memcapacitance. Likewise, equation (19) corresponds to the port relation $\phi = \mathcal{M}_C(\sigma)\,q$ of a charge-controlled memcapacitor.

Unlike memristor, two-terminal solid state memcapacitor is yet to be found. However, there are ongoing efforts to model the characteristics of memcapacitor for research, design and application purposes. Recently, an effort is made to demonstrate that the capacitance of a bilayer lipid membrane is indeed a memcapacitor because it shows the corresponding pinched hysteresis loop in the q-V plane [34]. So far, this is the only finding that reflects physical evidence of a memcapacitor. Furthermore, a mathematical model and its equivalent circuit of the bilayer lipid membrane memcapacitance were introduced [35]. The model helps to analyse the response and behaviour of the membrane memcapacitance. To model memcapacitor, it is important to note that there are classes of memcapacitors, just like in the case of memristor.

The broader class of memcapacitor systems are referred to as memcapacitive systems. Furthermore, depending on which of the variables q or V acts as the independent source, there are voltage-controlled and charge-controlled memcapacitive systems. The general descriptions of a voltage-controlled and charge-controlled memcapacitive systems respectively, are given by the port and state equations as follows [4]:

$$\begin{cases} q(t) = M_C(x, V, t)\, V(t), \\ \dfrac{dx}{dt} = f(x, V, t)\,, \end{cases} \tag{20}$$

and

$$\begin{cases} V(t) = \mathcal{M}_C(x, q, t)\, q(t), \\ \dfrac{dx}{dt} = f(x, q, t)\,, \end{cases} \tag{21}$$

where M_C is the memcapacitance (memory capacitance) in Farad (F) and $\mathcal{M}_C$ is the memelastance (inverse of memcapacitance) measured in reciprocal farad (F^{-1}). The memcapacitance depends on the state variable of the system and the voltage, meanwhile the memelastance depends on the state of the system and the charge. Equations (20) and (21) are the generic descriptions of memcapacitive systems. However, an ideal voltage-controlled memcapacitor is the reduced forms of equations (20) by considering:

$$\frac{dx}{dt} = f(V, t) \;\; or \;\; x = \hat{h}(\phi, t).$$

Hence, it can be simply expressed as:

$$x = \int_{-\infty}^{t} V(\tau)\; d\tau = \phi\,(t).$$

Notice here that it is possible to have $\int_{-\infty}^{0} V(\tau)\; d\tau = 0$. Therefore, the port equation of the voltage-controlled memcapacitor becomes:

$$q(t) = \; M_C\,\langle \phi \rangle \cdot V(t). \tag{22}$$

Similarly, an ideal charge-controlled memcapacitor is the reduced form of equation (21) when the state variable of the system is just the function of the charge:

$$\frac{dx}{dt} = g(q, t) \;\; or \;\; x = \hat{h}(\sigma, t).$$

Recall that $\sigma(t) = \int_{-\infty}^{t} q(\tau)\; d\tau$ and it is possible to have $\sigma(0) = \int_{-\infty}^{0} q(\tau)\; d\tau = 0$, hence the port equation of a charge-controlled memcapacitor becomes:

$$V(t) = \mathcal{M}_C\langle \sigma \rangle \cdot q(t). \tag{23}$$

Similar to a memristor, the plot of q versus V and vice versa, of a memcapacitor is a pinched hysteresis loop in which for every value of V there are corresponding two values of q and vice versa, except at the origin. This is the requirement for assessing a model of memcapacitor. Equation (24) models a charge-controlled memcapacitor:

$$\begin{cases} V(t) = (\alpha_c\, x + \beta_c)\, q(t), \\ \dfrac{dx}{dt} = \gamma_c\, q(t), \end{cases} \tag{24}$$

where α_c, β_c and γ_c are the modelling parameters. This model is similar to the electronic model presented in [36] where the parameters α_c, β_c and γ_c are modeled by the values of the resistances and capacitances, hence the model can be integrated in SPICE as well. Here, the memelastance $\mathcal{M}_C = \alpha_c\, x + \beta_c$ and setting $\sigma(0) = \int_{-\infty}^{0} q(\tau)\; d\tau = 0$, the state equation (24) can be simplified to give:

$$x(t) = \gamma_c\, \sigma(t). \tag{25}$$

Substituting equation (25) into the port equation (24) and integrate with respect to time, it gives:

$$\phi(t) = \alpha_c \gamma_c \sigma^2(t) + \beta_c \sigma(t). \tag{26}$$

Given an exciting current as $I(t) = I_m\, cos(\omega t)$, the flowing charge becomes $q(t) = Q_m\, sin(\omega t)$ with its maximum value being Q_m. Therefore, given the values of the parameters α_c, β_c and γ_c the response of this model can be observed. For example, if $\alpha_c = 4F^{-1}$, $\beta_c = 1F^{-1}$ and $\gamma_c = 10C^{-1}s^{-1}$, and suppose that the flowing charge is expressed as $q(t) = Q_m\, sin\,(\omega t)$ with $Q_m = 0.5C$, the expressions for $\sigma(t)$, $x(t)$, $C^{-1}(x)$ and $V(t)$ could be determined accordingly. Figure 10 shows the response of the memcapacitor. Figures 10a and 10b show the charge-voltage waveform and the corresponding pinched hysteresis loop in the q-V plane. Figures 10c and 10d show the time-evolution of $\sigma(t)$ and the transitioning of the memelastance $\mathcal{M}_C(x)$. Hence, the results illustrate the signature of a memcapacitor. Unlike the presented model of memristor, here the state variable x is not bounded in the interval $[0, 1]$. Figure 11 shows the effect of increasing the applied input frequency and the pinched hysteresis loop in the q-V plane shrink to a linear graph.

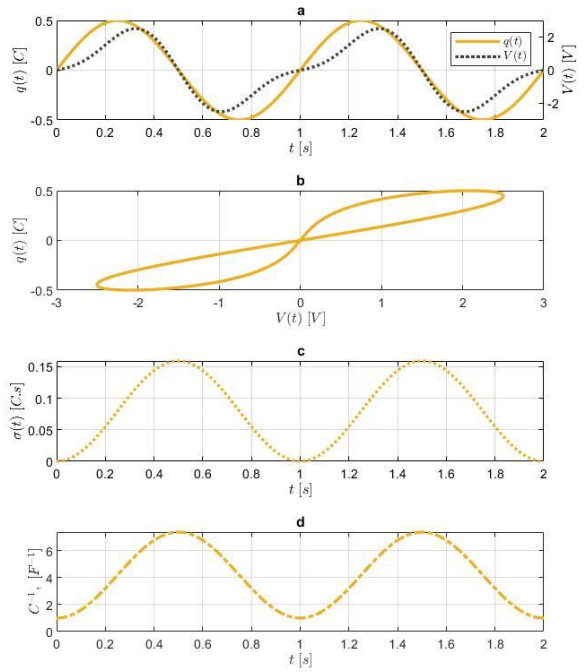

Figure 10: The response of the memcapacitor, (a) q-V waveform, (b) the corresponding pinched hysteresis loop in q-V plane, (c) time-evolution of σ and (d) the memelastance $\mathcal{M}_C$.

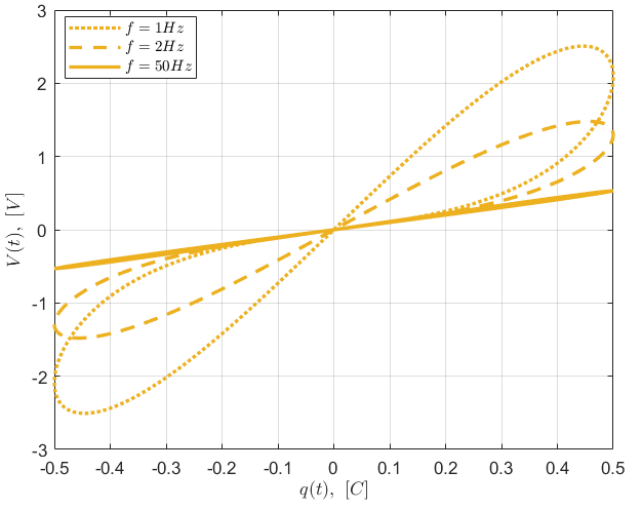

Figure 11: Effect of varying the applied input frequency on the response of memcapacitor. The pinched hysteresis loop shrinks to linear graph as the input frequency increases.

Although memcapacitor chips are yet to be built, there are many proposed models of memcapacitors enabling testing and validation of memcapacitor-based applications. Some of these models are built using voltage and current control sources, analogue passive and active components that can be integrated in SPICE circuit simulators from which the responsiveness of the model and its functionality could be assessed [37, 38]. Moreover, it includes circuit mutators and emulators [39]. In fact, there is remarkable progress in the simulation and testing of memcapacitor-based applications in various circuit simulators. It has been demonstrated that superconducting charge and flux quantum bits can indeed be classified as memcapacitive and meminductive systems, which unveils new futuristic potential of memelements in qubit-based devices and applications [40].

6. Meminductor

Recall that the constitutive relationship of an inductor L is given by $\phi = L \cdot I$ (or $d\phi = L\, dI$). Differentiating both sides of this equation, gives the port equation of an inductor as follows:

$$V(t) = \frac{d\phi}{dt} = \frac{d}{dt}\{L\, I\}. \tag{27}$$

For a time-invariant inductance, equation (27) is expressed as:

$$V(t) = L\frac{dI}{dt},$$

however, for a time-varying inductance, equation (27) could be expressed as:

$$V(t) = L\frac{dI}{dt} + I\frac{dL}{dt}.$$

Meminductor is the contraction of memory inductor and it is an inductor with memory whom inductance depends on the history of the flux across its terminals or current flowing through it. As explain in section 1, meminductor is defined by the constitutive relationship between ρ and q. Hence, depending on the mode of excitation, there are current-controlled and flux-controlled meminductors. Therefore, a current-controlled meminductor can described by the differentiable function: $\rho = \hat{\rho}(q)$. Differentiating both sides of theis equation, it becomes:

$$\frac{d\rho}{dt} = \frac{d}{dt}\big(\hat{\rho}(q)\big) = \frac{d\hat{\rho}(q)}{dq}\frac{dq}{dt}, \tag{28}$$

where $M_L(q) = \frac{d\hat{\rho}(q)}{dq}$ is the meminductance in Henry (H). Equation (28) describes the port relation $\phi = M_L(q)\, I$ of a current-controlled meminductor. Likewise, a flux-controlled meminductor can be described by a differentiable function $q = \hat{q}(\rho)$. Differentiating both sides of this equation becomes:

$$\frac{dq}{dt} = \frac{d}{dt}\big(\hat{q}(\rho)\big) = \frac{d\hat{q}(\rho)}{d\rho}\frac{d\rho}{dt}, \tag{29}$$

where $\mathcal{M}_L(\rho) = \frac{d\hat{q}(\rho)}{d\rho} = M_L^{-1}$ is the inverse-meminductance in per Henry (H^{-1}). Equation (29) correspond to the port relation $I = \mathcal{M}_L(\rho)\, \phi$ of a flux-controlled meminductor. Just like the other two memory circuit elements, there are different classes of meminductor. Therefore, the general port and state equations of a current-controlled meminductive system could be expressed as:

$$\begin{cases} \phi(t) = M_L(x, I, t)\, I(t), \\ \dfrac{dx}{dt} = f(x, I, t)\,, \end{cases} \tag{30}$$

and the equation set for flux-controlled meminductive system is expressed as:

$$\begin{cases} I(t) = \mathcal{M}_L(x, \phi, t)\ \phi(t), \\ \dfrac{dx}{dt} = f(x, \phi, t), \end{cases} \tag{31}$$

Ideal current-controlled and flux-controlled meminductors are specific case of equations (30) and (31) in which the state variables are just a functions of $I(t)$ and $\phi(t)$ respectively, such that: $x = \int_{-\infty}^{t} I(\tau)\ d\tau = q(t)$ and $x = \int_{-\infty}^{t} \phi(\tau)\ d\tau = \rho\ (t)$. Using the modelling techniques presented in [36], the equations set (32) models a meminductor:

$$\begin{cases} I(t) = (\alpha_L x + \beta_L)\ \phi(t), \\ \dfrac{dx}{dt} = \gamma_L\ \phi(t). \end{cases} \tag{32}$$

Where α_L, β_L and γ_L are modelling parameters and $\mathcal{M}_L = \alpha_L\ x + \beta_L$. Furthermore, the model (32) can be easily integrated in SPICE and the model parameters α_L, β_L and γ_L could be modelled by the values of resistors and capacitors. Hence, the model can be used for simulation of meminductor-based applications. Assuming $\rho(0) = \int_{-\infty}^{0} \phi(\tau)\ d\tau = 0$, the state equation in (32) is simplified to give:

$$x = \gamma_L\ \rho(t). \tag{33}$$

To observe the response of this model, consider an applied voltage $V(t) = V_0\ cos(\omega t)$, where V_0 is the voltage amplitude. Suppose $\phi(0) = \int_{-\infty}^{0} V(\tau)\ d\tau = 0$, then: $\phi(t) = \frac{V_0}{\omega}\ sin(\omega t)$ with its maximum value being $\frac{V_0}{\omega}$. Hence, the variables $\rho(t)$, $x(t)$ and $\mathcal{M}_L$ could be determined accordingly. Let the parameters $\alpha_L = 20H^{-1}$, $\beta_L = 1H^{-1}$ and $\gamma_L = 100Wb^{-1}s^{-1}$, the expressions for $\rho(t)$, $x(t)$ and $\mathcal{M}_L$ are determined accordingly, and the results are shown in Figure 12. The results show the typical I-ϕ waveform and the corresponding pinched hysteresis loop in the I-ϕ plane, the time-evolution of $\rho(t)$ and the inverse meminductance $\mathcal{M}_L$. The results confirmed the signatures of a meminductor. Figure 13 shows the effect of varying the input frequency on the response of memiductor.

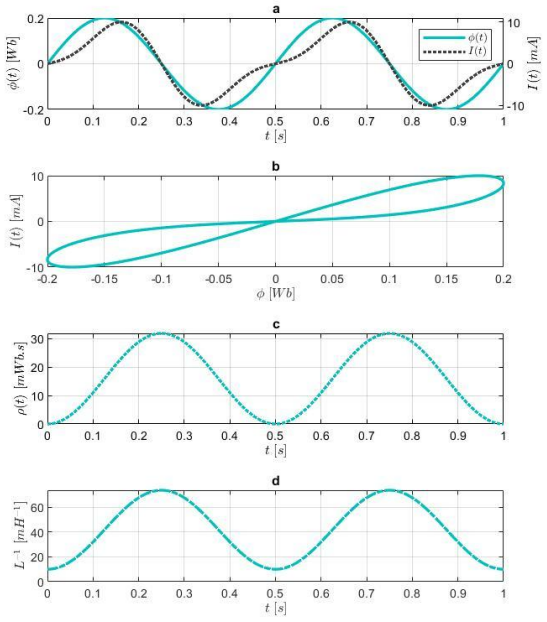

Figure 12: The response of the meminductor, (a) I-ϕ waveform, (b) pinched hysteresis loop in I-ϕ plane, (c) time-evolution of $\rho(t)$ and (d) the inverse meminductance L^{-1}.

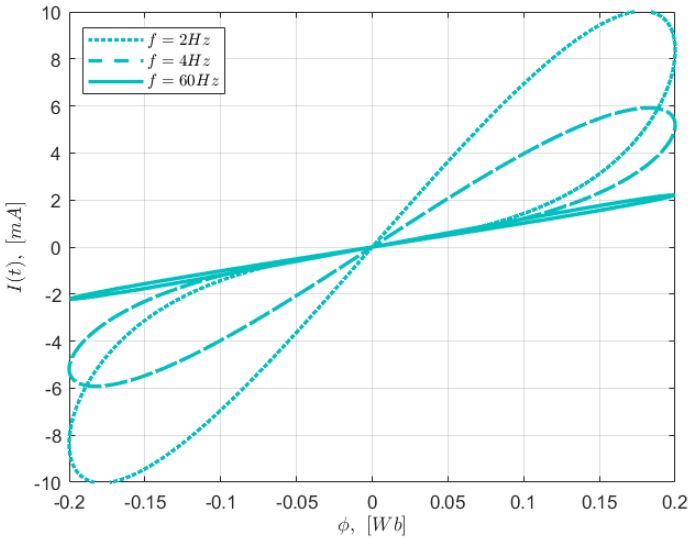

Figure 13: Effect of varying the applied input frequency on the response of meminductor. The lobe area of the pinched hysteresis loop shrinks and the curve becomes a linear graph as the input frequency increases.

Just like memcapacitor, a two-terminal solid state meminductor is yet to be discovered. So far, the only feasible effort for the physical realization of a meminductor is the findings presented in [41]. Notwithstanding, there are quite enormous published materials about the models of meminductor and its modelling techniques, including mutator and emulator circuits enabling design, testing and validation of meminductor-based applications [42, 43]. Meminductor emulators are potentially useful in the design and implementation of chaotic oscillators [44, 45].

7. Criticisms of Memelements

Every new scientific discovery is bounded to constructive criticisms, hence memelements are not an exception. The term memory resistor is already used by B. Widrow, however with the moniker *memistor* not *memristor* [46]. There are quite a number of discrepancies surrounding the proposed memristor by Chua [1] and the claimed one by HP Lab [12]. It is still debated on whether memristor is indeed the fourth passive circuit element, especially regarding its placement in the periodic table of circuit elements and the emergence of memcapacitor and meminductor. The claim of memristor as *the fourth fundamental passive circuit element* is problematic and there is called for the rejection of using such phrase [47]. From the charge-voltage perspective as clearly established in [47], the constitutive relationships for the three existing fundamental passive circuit elements R, C and L are $V = R\,\dot{q}$, $V = C^{-1}\,q$ and $V = L\,\ddot{q}$ respectively, with R, C and L being phenomenological constants denoting resistance, capacitance and inductance. Notice here that the dots atop the charge q represent derivative with respect to time, i.e. $\dot{q} = \frac{dq}{dt}$, $\ddot{q} = \frac{d^2q}{dt^2}$ and so on. Instead of using periodic table in the α-β domain as illustrated in Figure 2, here the periodic table is based on the ϕ-q and V-q plane depending on the nature of the associated field. Using Faraday's law $V = -\frac{d\phi}{dt}$ and Ampere's law, allow to formulate a periodic table of circuit elements in charge-flux and charge-voltage domains, as illustrated in Figure 14.

The periodic table of circuit elements Figure 14 consists of rows and columns forming grids with q along the vertical-axis and V (and ϕ) along the horizontal-axis. Each slot corresponds to a particular circuit element, the discovered ones are labelled and others yet to be discovered are left blank. By the way, some of the blank slots are meaningless because there are no satisfying constitutive relationships and some can be occupied by active circuit elements that in future may be discovered. The letters A, B, C, D and W, X, Y, Z at the left and top of the table are for slot referencing. Inspectingly, the relations for each of the known fundamental circuit

element (C, R and L) spreads diagonally as indicated by the diagonal arrows accordingly. In the charge-voltage domain, fundamental elements do not spread to column Z, hence they are situated in column Y (marked by the big box) with their constitutive relationships expressed in terms of the variables V and q. Stationary charges cannot produce magnetism, therefore only inductor and resistor exist in the ϕ-q domain [47]. Hence, memristor does not exist in the charge-flux domain.

Looking at Figure 14, the CR information asserted by Chua [28] [1], is located in slots (A,Y), (A,Z), (B,Y) and (B,Z) for capacitor, memristor, resistor and inductor respectively, demarcated by the big dotted rectangle. Hence the proposed memristor by Chua and HP is located in slot A,Z. Interestingly, Isaac Abraham [47], demonstrated that the only possible slots for the existence of memristor on the V-q periodic table are A,Z and D,Y. However, the slot A,Z is already occupied by simple linear resistor and the occupant of slot D,Y must be active and non-fundamental which violates the claim of memristor as passive and fundamental circuit element.

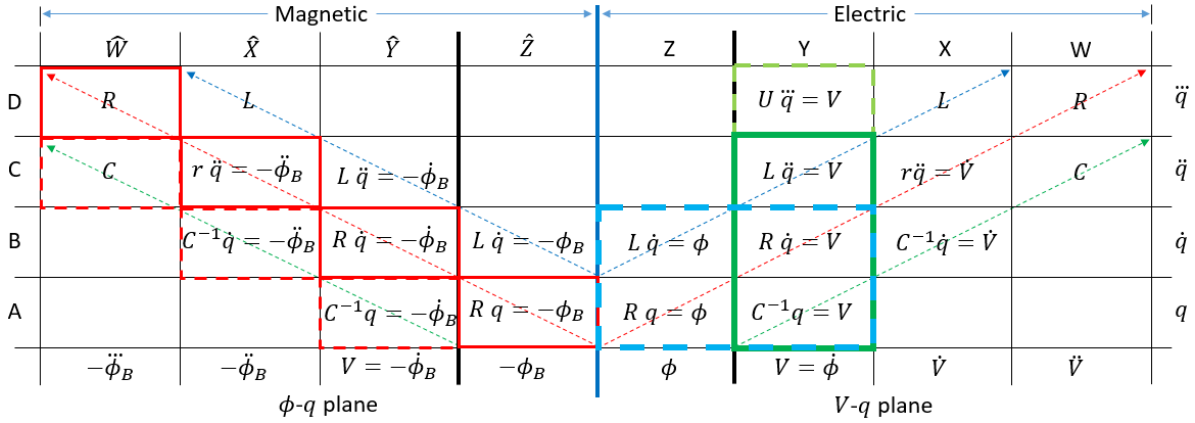

Figure 14: Periodic table of circuit element in charge-flux (ϕ-q) and charge-voltage (V-q) domains.

Another issue with the found memristor is the absent of magnetism in which the theorized variable ϕ is not representing the actual magnetic flux [48, 26]. It is concluded that the postulated memristor in 1971 has not been found and likely impossible [26]. Recall that one of the reasons to call memristor as *fundamental passive circuit element* is due to the claim that it cannot be realized by simple combination of the three existing fundamental passive circuit elements. However, memristor is locally active as can be observed from its governing equations. Hence, it is suggested that the Chua's general proof of memristor as passive is invalid because it violates the second law of thermodynamic [49]. Furthermore, Dimitri et al. have proved that the ideal memcapacitors and meminductors are not passive or cyclo-passive devices, adding that they are non-physical devices [50]. Therefore, their modelling and realizability as physical-device is highly debatable. Other critiques of memristor are the violation of Landauer's principle, etc. [51, 52].

There are many other issues surrounding the understanding of memristors to the extent that even the pioneer tends to be confused. For example, Chua asserted that all two-terminal non-volatile resistance switching memories are memristors [53], however it is reported experimentally that resistance switching memories are indeed not memristors [54]. Notice however that Chua's assertion of resistance switching memory cells as memristors was based on their exhibit pinched hysteresis loop. Notwithstanding, there are many existing phenomena with pinched hysteresis loop that are not memristors [55]. Lastly, Pershin et al. proposed a simple test to experimentally prove whether a given device is indeed memristor or not [56], however this method is not enough. Recently, they improved the method along with test experiment disproving *Φ-memristor* as memristor [57]. Finally, Pershin et al. have extensively demonstrated that *memelements* are not fundamental circuit elements, but they are rather the extensions of resistors, capacitors and inductors in response to their memory effects [58].

Normally, a physical system does not immediately respond to an external perturbation. Any device subjected to perturbation possesses some degree of memory effects and the extent to which the memory can be detected depends on the type of the system [58]. A system can be regarded as memoryless if its degree of memory is not detectable. Unlike the fundamental circuit elements (R, L, C), memelements are systems whose memory can be detected under specific experimental conditions. In fact, any device describe by the set of equations (34) will show some degree of memory effects.

$$\begin{aligned} y(t) &= H(x,u,t)\,u(t), \\ \frac{dx}{dt} &= F(x,u,t). \end{aligned} \tag{34}$$

Here, $u(t)$ and $y(t)$ are finite observable quantities and they are respectively, the input and output of the system, meanwhile H is a generalized response function. Therefore, $u(t)$ and $y(t)$ can be measured directly, but H can only be obtained indirectly, thus demonstrating the response of the system. Moreover, F is a bounded function in x which determines its evolution with respect to time. It is quite clear that for x being dynamic and also representing the set of internal state variable of the system, anytime the system is subjected to perturbation (say at time t_0) or any intermediate time, there will be change of state which happens at a later time (say, t'), and this is the manifestation of the memory effects. The response function H depends strongly on the bounded function F because it is what determined the dynamic of the state variable x.

Exploring equation (34), we see that for a basic linear resistor, $y(t) = V$, $u(t) = I$ and $H(x,u) = R$, implying that $R = \frac{V}{I}$. However, if the state equation is taken into account, then it becomes $R(x,I) = \frac{V}{I}$, thus manifesting the memory effect of a resistor having quantity resistance $R(x,I)$. Likewise, for a basic linear capacitor, $y(t) = q$, $u(t) = V$ and $H(x,u) = C$, implying that $C = \frac{q}{V}$. To include the memory response of a capacitor, equation (34) can give $C(x,V) = \frac{q}{V}$. Similarly, for a basic linear inductor, $y(t) = \phi$, $u(t) = I$ and $H(x,u) = L$, thus satisfying $L = \frac{\phi}{I}$. Taking into account the memory response of an inductor, equation (34) becomes $L(x,I) = \frac{\phi}{I}$. Therefore, the response function $H(x,u)$ defines the quantities $R(x,I)$, $C(x,V)$ and $L(x,I)$ which expresses that under the appropriate experimental conditions, resistances, capacitances and inductances display some degree of memory effect. Hence, the set of equations (34) gives the description of a memelement, and certainly not fundamental, implying that memelements are extensions of resistors, capacitors and inductors, thus reflecting their memory effect. Now it becomes clear that linear resistors, capacitors and inductors are the only three fundamental circuit elements. Table 1 summarizes some attributes comparing fundamental circuit elements and memelements.

Table 1: Comparison of some specific attributes of fundamental circuit elements with memelements.

Attributes	Fundamental circuit elements (R, L, C)	Memelements (M_R, M_C, M_L)
Mathematical description	Linear relationship	Nonlinear relationship
Nature	Fundamental	Composite
Physicality	Physical	Unphysical
Realizability as fundamental	Realizable	Highly unlikely
Passivity	Passive	Debatable
Input frequency dependent	Dependent	Highly dependent
Modelling	Simple	Complex
Criticisms	Less critical	Highly critical
Scalability	Micro	Nano
Hardware implementation	Simple	Complex
Degree of memory effect	Undetectable	Detectable
Port response	Linear characteristic	Pinched hysteresis loop
Ideality	feasible	Unlikely/Conceptual
Landauer's principle	Satisfiable	Unsatisfiable
Second law of Thermodynamic	Satisfiable	Unsatisfiable

The oppositions to the concept of memristor and the called for its rejection as the fourth fundamental passive circuit element do not affect its potential as promising component for amazing computing and memory applications. Likewise, memcapacitor and meminductor may not exist as fundamental circuit elements, but their concepts are phenomenal in terms of applications, as mention in the following.

8. Applications of Memelements

Despite the many oppositions and criticisms surrounding the existence and concepts of memelements, there are quite huge number of published materials and reports on their phenomenal applications in various facets of electronic systems and designs, these include both analogue and digital domains, discrete and array configurations [6, 59]. However, there are challenges when it comes to applying memelements much of which have to do with their device physics that are currently under study and chips availability for purchase to enable testing and implementation for evaluating their functionalities in an undertaken project. Many researchers built in-house memelements for their experimental purposes. The following presents some key applications of memelements, thus enabling positive reverberation in exploring the potential of these circuit elements.

Chaotic circuits: Among the many reported application areas of memelements are in chaotic systems. There are many proposed models of memcapacitor and meminductor based chaotic circuits including validation by experimental implementations [60, 61, 62, 63, 64, 65, 66]. The analysis of these models allows to study the complex dynamic characteristics such as attractors, bifurcation, multistability and Lyapunov exponents. Lai et al. presents an interesting collection of memelements-based chaotic systems, enabling modeling, dynamical analysis, control and circuit realization [67]. The collection presents state of the art and future directions for further study on the potential of memelements in chaotic systems and hardware circuit design. This is done as an effort to address the three main challenges in this research area, namely:

- How to generate special chaotic systems, and this can be achieved through modelling.
- How to detect and show the complex dynamics of chaotic systems, and this can be performed through analysis.
- How to control the chaotic systems to target a desired behaviour, and this can be achieved through control and circuit realization.

Therefore, readers who are interested in chaos and chaotic systems are encourage to check up these references.

Nonvolatile memory: One of the key features of memory circuit elements is their memory capability and they are very useful in digital memory applications, digital logic circuits and hybrid field programmable gate arrays (FPGA) [68]. Memristor crossbar arrays are compatible with CMOS (complementary metal oxide semiconductor) technology allowing to create multi-layer crossbar with increased integration density of memristive devices enabling large storage application. Not only capable of achieving stack of crossbar arrays, memristor crossbars support in-memory computing which is essential feature for artificial intelligence due to the required large number of data communication and storage [69]. Strukov and Williams proposed a topological framework, a powerful electronic circuit architecture enabling to construct multilayer crossbar arrays with significantly increased integration density of memristive crosspoint devices [68]. This proposal is quite interesting because it promises further downsizing beyond the scaling limits of lateral feature sizes. The findings by Li et al. showed an encouraging step forward to implementing multilayer memristor crossbar arrays for memory application, signal processing and edge detection [69].

Neuromorphic systems: Nowadays, data communication latency and large storage requirements in contemporary technological scale are the main challenges facing Von Neumann machine architecture. Hence, this is referred to as the bottleneck of von Neuman architecture. Additionally, there are concerns that Moore's law is approaching its dead end owing to the fact that the smallest transistor is infinitesimally few nano-meter in size, thus posing a challenge to further downsizing, thanks to memristor nano scalability. Memristor is a promising option for memory devices owing to its unique intrinsic device-level properties, enabling both storing and in-memory computing, that are desperately needed to alleviate the bottleneck in Von Neumann

computing architecture. The conductance modulation of memristor resembles that of a chemical synapse, thus it allows memelements to be used in the electronic modeling of biological synapse [70, 71, 72, 73]. The features of memelements such as nano-scalability and conductance modulation couple with their memory capability, these devices are phenomenal in neuromorphic computing enabling the design and implementation of brain-like chips [74]. The memelements-based neuromorphic chips show promising processing power with good energy efficiency. Using the concept of electron shielding, it has been demonstrated that memcapacitive crossbar arrays can perform parallel multiply-accumulate operations which is promising in neuromorphic computing based on artificial neural networks [75]. There is great progress in the design and implementation of memristor-based artificial neural networks. Aguirre et al. presented an interesting review on the design and implementation of hardware-based memristive artificial neural networks (ANNs), detailing different design techniques along with their advantages and disadvantages, and the general assessment of the performance metric [76].

Image and Signal processing: The connection flexibility of memory circuit elements allows to design various system architectures including crossbar array configurations. For example, memristor crossbars demonstrate reliable energy-efficient hardware implementation for analogue signal and image processing, edge computing, convolutional image filtering and IoT [77]. An experiment is conducted using memristors to detect auditory cues in rat brain [78]. This is encouraging for those interested in memristor for signal processing in bio-medical applications.

Memelements are also applicable to programmable analog logic circuits, amplitude and frequency modulation, learning circuits, quantum computing and many other applications.

9. Conclusion

For enhanced comprehension of memelements, an insight into these circuit elements is presented, including their existence criticisms, modeling techniques and potential applications. Axiomatically, the three existing fundamental passive circuit elements are resistor, capacitor and inductor. The memelements, namely, memristor, memcapacitor and meminductor manifest the memory effects of their respective parent elements. Hence, they are extensions of the three fundamental circuit elements. Unlike fundamental circuit elements, memelements are not passive elements but rather locally active which is also the manifestation of their hysteretic behavior. Therefore, given the references, it is well established that memelements are neither fundamental nor passive circuit elements. The common signature of memelements is a pinched hysteresis loop in the governing plane of their constitutive variables with its lobe area decreases with increase in the input frequency. At high input frequency, memristor resembles ordinary resistor. The presented models of memcapacitor and meminductor could be built electronically, hence they can be used for testing and simulation purposes, both in circuit simulators and theoretical analysis.

The paper further highlighted some key application areas of memelements, especially in nonvolatile memories and computing architectures for brain-inspired networks. Von Neumann architecture cannot withstand the significant increase in computing power due to the memory requirements and large data communication by the recent advancements in data-intensive, big-data problems, artificial intelligence (AI) and so on. This drawback is considered as the bottleneck of Von Neumann computing. In an effort to resolve the bottleneck in Von Neumann architecture, some computing techniques are used, such as intense parallelism with the aid of cache memory and near memory computing. However, in-memory computing and parallel processing are the solutions to the Von Neumann bottleneck. Thanks to the in-memory computing capability of memristor-based architectures. The memristor crossbars have been proven to be reliable replacement of Von Neuman architecture mainly because of two reasons. Firstly, memristor is a nano component with excellent nano-scalability (miniaturization) allowing to create large storage of relatively small physical size. Hence the power consumption is very much lower. Secondly, memristor crossbars allow in-memory computing thereby improving the data communication latency between the memory unit and the processing unit. Therefore, these capabilities allow memristor crossbar architectures to have a better computing power with improved efficiency. Apparently, there are much to be explored in the future regarding the continuous efforts toward realization of memelements' chips and their impactfulness in the design and implementation of very reliable and sophisticated systems.

10. References

[1] Chua, L.O, "Memristor-the missing circuit element.," *IEEE Transactions on circuit theory,* vol. 18, p. 507–519, 1971.

[2] Isah, A. Nguetcho, A.T, Binczak, S and Bilbault, J.M, "Dynamics of a charge-controlled memristor in master–slave coupling," *Electron. Lett.,* vol. 56, p. 211–213, 2020.

[3] Chua, L. O. and Kang, S. M., "Memristive devices and systems," *Proc. IEEE,* vol. 64, p. 209–223, 1976.

[4] Di Ventra, M., Pershin, Y. V. and Chua, L. O., "Circuit elements with memory: memristors, memcapacitors, and meminductors," *Proceedings of the IEEE,* vol. 97, no. 10, pp. 1717-1724, 2009.

[5] Yin, Z. Tian, H., Chen, G. and Chua, L.O., "What are memristor, memcapacitor, and meminductor?," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 62, no. 4, pp. 402-406., 2015.

[6] Pershin, Y.V. and Di Ventra, M., "Memory effects in complex materials and nanoscale systems," *Adv. Phys.,* vol. 60, p. 145–227, 2011.

[7] Pershin, Y.V., Martinez-Rincon, J. and Di Ventra, M., "Memory circuit elements: from systems to applications," *J. Comput. Theor. Nanosci.,* vol. 8, p. 441–448, 2011.

[8] Adhikari, S., Sah, M., Kim, H. and Chua, L.O., "Three fingerprints of memristor," *IEEE Transactions on Circuits and Systems I: Regular Paper,* vol. 60, p. 3008–3021., 2013.

[9] Biolek, D., Biolek, Z., Biolková, V. and Kolka, Z., "Some fingerprints of ideal memristors.," in *IEEE international symposium on circuits and systems (ISCAS2013)*, 2013.

[10] Lin, D., Chua, L. O. and Hui, S.-Y., "The first man-made memristor: Circa 1801 [scanning our past]," *Proc. IEEE,* vol. 103, p. 131–136, 2014.

[11] Kumar, M. J., "Memristor–why do we have to know about it?," *IETE technical review,* vol. 26, no. 1, pp. 3-6, 2009.

[12] Strukov, D., Snider, G., Stewart, D. and Williams, S.R., "The missing memristor found," *nature,* vol. 453, no. 7191, pp. 80-83, 2008.

[13] Williams, R.S., "How we found the missing memristor," *IEEE spectrum,* vol. 45, pp. 28-35, 2008.

[14] Isah, A., Nguetcho, A.S.T., Binczak, S. and Bilbault, J.M., "Polarity reversal effect of a memristor from the circuit point of view and insights into the memristor fuse," *Front. Commun. Networks 2,* vol. 2, p. 647528, 2021.

[15] Manouras, V., Stathopoulos, S., Serb, A. and Prodromakis, T., "Selectively biased tri-terminal vertically-integrated memristor configuration," *Sci. Reports,* vol. 12, p. 10467, 2022.

[16] Chua, L.O., "Everything you wish to know about memristors but are afraid to ask," *Radioengineering,* vol. 24, p. 319, 2015.

[17] Nugent, A., "knowm SDC-memristor," Knowm Inc, [Online]. Available: www.knwom.com.

[18] Yoshida, C., Kurasawa, M., Lee, Y.M., Aoki, M. and Sugiyama, Y., "Unipolar resistive switching in cofeb/ mgo/ cofeb magnetic tunnel junction," *Appl. Phys. Lett.,* vol. 92, 2008.

[19] Yanagida, T., Nagashima, K., Oka, K., Kanai, M., Klamchuen, A., Park, B. H., and Kawai, T.,"Scaling effect on unipolar and bipolar resistive switching of metal oxides," *Sci. reports,* vol. 3, p. 1657, 2013.

[20] Huang, H.-H., Shih, W.-C. and Lai, C.-H., "Nonpolar resistive switching in the pt/mgo/pt nonvolatile memory device," *Appl. Phys. Lett.,* vol. 96, 2010.

[21] Yin L., Cheng R., Wang Z., Wang F., Sendeku M.G., Wen Y., Zhan X., He J., "Two-dimensional unipolar memristors with logic and memory functions," *Nano letters,* vol. 20, p. 4144–4152, 2020.

[22] Linn, E., Rosezin, R., Kügeler, C. and Waser, R., "Complementary resistive switches for passive nanocrossbar memories," *Nat. materials,* vol. 9, p. 403–406, 2010.

[23] Wang Z., Joshi S., Savel'ev S.E., Jiang H., Midya R., Lin P., Hu M., Ge N., Strachan J.P., Li Z., and Wu Q., "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nat. materials,* vol. 16, p. 101–108, 2017.

[24] Isah, A., Umar, F. A. and Bilbault, J.M., "The significance of a window function in the modeling of HP TiO2 memristor: Pros and Cons," *Journal of Sustainable Engineering and Technology,* vol. 1, no. 2, pp. 117-128, 2024.

[25] Isah, A. and Bilbault, J.M., "Review on the basic circuit elements and memristor interpretation: Analysis, technology and applications," *J. Low Power Electron. Appl. 12, 44 (2022).,* vol. 12, p. 44, 2022.

[26] Vongehr, S. and Meng, X., "The missing memristor has not been found," *Sci. reports,* vol. 5, p. 11657, 2015.

[27] Chandra, S., "On the discovery of a polarity-dependent memory switch and/or memristor (memory resistor).," *IETE Tech. Rev.,* vol. 27, p. 179–180, 2010.

[28] Chua, L. O., "Nonlinear circuit foundations for nanodevices. i. the four-element torus," *Proc. IEEE.* , vol. 91, p. 1830–1859, 2003.

[29] Chua, L. O., "Device modeling via nonlinear circuit elements," *IEEE Transactions on Circuits Syst.,* vol. 27, p. 1014–1044, 1980.

[30] Biolek, Z., Biolek, D., Biolková, V. and Kolka, Z., "All pinched hysteresis loops generated by (α, β) elements: In what coordinates they may be observable," *IEEE Access,* vol. 8, p. 199179–199186, 2020.

[31] Ghosh, S., Bera, A.K. and Das, S., "Evidence for nonlinear capacitance in biomembrane channel system," *J. theoretical biology,* vol. 200, p. 299–305, 1999.

[32] Kumar, J., Gupta, P.D. and Ghosh, S., "Effects of nonlinear membrane capacitance in the hodgkin-huxley model of action potential on the spike train patterns of a single neuron," *Europhys. Lett.,* vol. 142, p. 67002, 2023.

[33] Santos-Sacchi, J. and Tan, W., "Complex nonlinear capacitance in outer hair cell macro-patches: effects of membrane tension," *Sci. Reports,* vol. 10, p. 6222, 2020.

[34] Najem J.S., Hasan M.S., Williams R.S., Weiss R.J., Rose G.S., Taylor G.J., Sarles S.A., Collier C.P., "Dynamical nonlinear memory capacitance in biomimetic membranes," *Nat. communications,* vol. 10, p. 3239, 2019.

[35] Smirnova, E.Y. and Anosov, A.A., "Bilayer lipid membrane as memcapacitance: Capacitance–voltage pinched hysteresis and negative insertion conductance," *Membranes,* vol. 13, p. 97, 2023.

[36] Yuan, F. and Li, Y., "A chaotic circuit constructed by a memristor, a memcapacitor and a meminductor," *Chaos: An Interdiscip. J. Nonlinear Sci.,* vol. 29, 2019.

[37] Biolek, D., Biolek, Z. and Biolkova, V., "Spice modeling of memristive, memcapacitative and meminductive systems. In," in *2009 European conference on circuit theory and design, 249–252*, 2009.

[38] Biolek, D., Biolek, Z. and Biolkova, V., "Spice modelling of memcapacitor," *Electron. letters,* vol. 46, p. 520, 2010.

[39] Romero, F. J., Ohata, A., Toral-Lopez, A., Godoy, A., Morales, D. P., and Rodriguez, N., "Memcapacitor and meminductor circuit emulators: A review," *Electronics,* vol. 10, p. 1225, 2021.

[40] Shevchenko, S. N., Pershin, Y. V. and Nori, F., "Qubit-based memcapacitors and meminductors," *Phys. Rev. Appl.,* vol. 6, p. 014006, 2016.

[41] Dinavahi, A., Yamamoto, A. and Harris, H. R., "Physical evidence of meminductance in a passive, two-terminal circuit element," *Sci. Reports,* vol. 13, p. 1817, 2023.

[42] Biolek, D., Biolek, Z. and Biolkova, V., "Pspice modeling of meminductor," *Analog. Integr. Circuits Signal Process,* vol. 66, p. 129–137, 2011.

[43] Romero, F. J., Escudero, M., Medina-Garcia, A., Morales, D. P. and Rodriguez, N., "Meminductor emulator based on a modified antoniou's gyrator circuit," *Electronics,* vol. 9, p. 1407, 2020.

[44] Wang, X., Yu, J., Jin, C., Iu, H. H. C. and Yu, S., "Chaotic oscillator based on memcapacitor and meminductor," *Nonlinear Dyn.,* vol. 96, p. 161–173, 2019.

[45] Xu, B., Wang, G., Iu, H. H.-C., Yu, S. and Yuan, F., "A memristor–meminductor-based chaotic system with abundant dynamical behaviors," *Nonlinear Dyn.,* vol. 96, p. 765–788, 2019.

[46] Widrow, B., "Adaptive" adaline" Neuron Using Chemical" memistors."," Stanford Electronics Laboratories, 1960, pp. 1553-1552.

[47] Abraham, I., "The case for rejecting the memristor as a fundamental circuit element," *Sci. reports,* vol. 8, p. 10972, 2018.

[48] Vongehr, S., "Missing the memristor," *Adv. Sci. Lett.,* vol. 17, p. 285–290, 2012.

[49] Sundqvist, K. M., Ferry, D. K. and Kish, L. B., "Memristor equations: incomplete physics and undefined passivity/activity," *Fluctuation Noise Lett.,* vol. 16, p. 1771001, 2017.

[50] Jeltsema, D. and van der Schaft, A., "Ideal memcapacitors and meminductors are overunity devices," *Sci. reports,* vol. 10, p. 16688, 2020.

[51] Meuffels, P. and Soni, R., "Fundamental issues and problems in the realization of memristors," arXiv preprint arXiv:1207.7319, 2012.

[52] Jeltsema, D., "Memristors: The rise and the fall (?)," in *21st International Symposium on Mathematical Theory of Networks and Systems*, 2014.

[53] Chua, L.O., "Resistance switching memories are memristors," in *Handb. memristor networks*, Springer, 2019, p. 197–230.

[54] Kim, J., Pershin, Y. V., Yin, M., Datta, T. and Di Ventra, M., "An experimental proof that resistance-switching memory cells are not memristors," *Adv. Electron. Mater.,* vol. 6, p. 2000010, 2020.

[55] Upadhyaya, H. M. and Chandra, S.,, "Polarity-dependent memory switching effects in the ti/cdxpb1-xs/ag system," *Semicond. Sci. Technol.,* vol. 10, p. 332, 1995.

[56] Pershin, Y.V. and Di Ventra, M., "A simple test for ideal memristors," *J. Phys. D: Appl. Phys.,* vol. 52, p. 01LT01, 2018.

[57] Pershin, Y. V., Kim, J., Datta, T. and Di Ventra, M., "An experimental demonstration of the memristor test," *Phys. E: Low-dimensional Syst. Nanostructures,* vol. 142, p. 115290, 2022.

[58] Di Ventra, M. and Pershin, Y.V., Memristors and Memelements: Mathematics, Physics and Fiction, Springer Nature, 2023.

[59] Mazumder, P., Kang, S.-M. and Waser, R., "Memristors: devices, models, and applications," *Proc. IEEE,* vol. 100, p. 1911–1919, 2012.

[60] Liu, X., Bi, X and Yan, H. M. J., "A chaotic oscillator based on meminductor, memcapacitor, and memristor," *Complexity,* p. 7223557, 2021.

[61] Abro, K.A. and Atangana, A., "Numerical study and chaotic analysis of meminductor and memcapacitor through fractal fractional differential operator," *Arab. J. for Sci. Eng.,* vol. 46, p. 857–871, 2021.

[62] Wang, G.-Y., Cai, B.-Z., Jin, P.-P. and Hu, T.-L.,, "Memcapacitor model and its application in a chaotic oscillator," *Chin. Phys. B,* vol. 25, p. 010503 (2015)., 2015.

[63] Liu, X., Mou, J., Wang, J., Banerjee, S. and Li, P., "Dynamical analysis of a novel fractional-order chaotic system based on memcapacitor and meminductor," *Fractal Fract.,* vol. 6, p. 671, 2022.

[64] Yuan, F., Wang, G. and Wang, X., "Chaotic oscillator containing memcapacitor and meminductor and its dimensionality reduction analysis," *Chaos: An Interdiscip. J. Nonlinear Sci.,* vol. 27, 2017.

[65] Zhao, Q., Wang, C. and Zhang, X., "A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit," *Chaos: An Interdiscip. J. Nonlinear Sci.,* vol. 29, 2019.

[66] Guo, M., Yang, R., Zhang, M., Liu, R., Zhu, Y., and Dou, G., "A novel memcapacitor and its application in a chaotic circuit," *Nonlinear Dyn.,* vol. 105, p. 877–886, 2021.

[67] Lai, Q., Bao, B., Chen, C., Kengne, J. and Akgul, A., "Circuit application of chaotic systems: modeling, dynamical analysis and control," *The European Physical Journal Special Topics,* vol. 230, pp. 1691-1694, 2021.

[68] Strukov, D. B. and Williams, R. S., "Four-dimensional address topology for circuits with stacked multilayer crossbar arrays," *Proc. Natl. Acad. Sci.,* vol. 106, p. 20155–20158, 2009.

[69] Li C., Wang Z., Rao M., Belkin D., Song W., Jiang H., Yan P., Li Y., Lin P., Hu M. and Ge N., "Long short-term memory networks in memristor crossbar arrays," *Nat. Mach. Intell.,* vol. 1, p. 49–57, 2019.

[70] Cai, W. and Tetzlaff, R., "Synapse as a memristor," in *Handb. Memristor Networks*, Springer, 2019, p. 351–367.

[71] Zhao L., Fan Z., Cheng S., Hong L., Li Y., Tian G., Chen D., Hou Z., Qin M., Zeng M. and,Lu X., "An artificial optoelectronic synapse based on a photoelectric memcapacitor," *Adv. Electron. Mater.,* vol. 6, p. 1900858, 2020.

[72] Zhang, H., Liu, R., Zhao, H., Sun, Z., Liu, Z., He, L. and Li, Y., "Research progress of biomimetic memristor flexible synapse," *Coatings,* vol. 12, p. 21, 2021.

[73] Li Y., Zhong Y., Zhang J., Xu L., Wang Q., Sun H., Tong H., Cheng X. and Miao X.,"Activity-dependent synaptic plasticity of a chalcogenide electronic synapse for neuromorphic systems," *Sci. reports,* vol. 4, p. 4906, 2014.

[74] Duan X., Cao Z., Gao K., Yan W., Sun S., Zhou G., Wu Z., Ren F. and Sun B., "Memristor-based neuromorphic chips," *Adv. Mater.,* vol. 36, p. 2310704, 2024.

[75] Demasius, K.-U., Kirschen, A. and Parkin, S., "Energy-efficient memcapacitor devices for neuromorphic computing," *Nat. Electron.,* vol. 4, p. 748–756, 2021.

[76] Aguirre F., Sebastian A., Le Gallo M., Song W., Wang T., Yang J.J., Lu W., Chang M.F., Ielmini D., Yang Y. and Mehonic A., "Hardware implementation of memristor-based artificial neural networks," *Nat. communications,* vol. 15, p. 1974, 2024.

[77] Li C., Hu M., Li Y., Jiang H., Ge N., Montgomery E., Zhang J., Song W., Dávila N., Graves C.E. and Li Z., "Analogue signal and image processing with large memristor crossbars," *Nat. electronics,* vol. 1, p. 52–59, 2018.

[78] Sbandati C., Stathopoulos S., Foster P., Peer N.D., Sestito C., Serb A., Vassanelli S., Cohen D. and Prodromakis T., "Single-trial detection of auditory cues from the rat brain using memristors," *Sci. Adv.,* vol. 10, no. 36, p. eadp7613, 2024.